AMENDMENTS TO THE SPECIFICATION

1. Please replace the second paragraph of the Summary of Invention with the following amended paragraph:

Briefly summarized, a frequency divider dividing an original clock to form a target clock with a frequency factor M being a positive odd number includes a front set circuit, a middle set circuit and a rear set circuit. The front set circuit includes a first clock generator with a clock input end connected to a trigger clock having a frequency the same as that of the original clock and a trigger phase, and a first logic gate with a first input end connected to an output end of the first clock generator, and a second input end connected to a signal input end of the first clock generator. The middle set circuit includes a second clock generator with a clock input end connected to the trigger clock, and (M-~~1~~3)/2 serially connected first sets of clock generators with a clock input end of each first set of clock generators connected to the trigger clock, a signal input end of the immediately previous clock generator within the (M-~~1~~3)/2 first sets of clock generators connected to an output end of the first logic gate in the front set circuit, and an output end of the last clock generator within the (M-~~1~~3)/2 first sets of clock generators connected to a signal input end of the second clock generator in the middle set circuit. And the rear set circuit includes a third clock generator with a clock input end connected to the trigger clock, and a signal input end connected to an output end of the second clock generator in the middle set circuit, and a second logic gate with a first input end connected to an output end of the third clock generator in the rear set circuit, a second input end connected to the output end of

the second clock generator in the middle set circuit, and an output end for outputting the target clock.